Design of a low-jitter, low-power, radiation robust PLL with BIST features

José Pedro Cardoso – on-going, supervisor José Machado da Silva

ACEOLE
www.cern.ch/aceole

INESCPORTO
U PORTO
FEUP FACULDADE DE ENGENHARIA UNIVERSIDADE DO PORTO

- The GBTX Project" is part of the LHC "Radiation Hard Optical Link Project (http://cern.ch/proj-gbt), aiming the design of low-noise, radiation tolerant circuits in 130 nm CMOS technology. In particular, a very low-power, low phase noise PLL in order to:
  - Reduce the jitter in digital communication data (output Jitter < 15 ps pk-pk; locking range of ± 8 kHz for an incoming signal 40.0786 MHz)
  - Generate a clean clock to other blocks of the project
  - Two operating modes: PLL (jitter filtering) or autonomous oscillator
  - Auto-Calibration, Calibration and Self-Test capabilities

Description

- Radiation tolerant low-power and low-noise PLL with the possibility of operation in either strong, or close to, weak inversion.
- Built-in features for calibration, self-calibration, automatic gain control and BIST blocks,
- Possibility of the extension of the BIST to Burn In on-chip, using dissipative elements to create a controlled stress by temperature. This would save some tests usually done with ATEs.

- The increasing phase noise of the circuit, due to the power reduction, is filtered by the high Q resonator on the circuit (Quartz Crystal)
- There is a trade-off in the behaviour of the PLL when operating in weak inversion subject to radiation and in a radiation free environment. This aspect is being explored to operate as close to the weak inversion as possible.